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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,295	11/21/2001	Ton Engbersen	CH919980050-US1	3838

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EXAMINER	
NGUYEN, TOAN D	
ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/991,295	ENGBERSEN ET AL.
	Examiner	Art Unit
	Toan D Nguyen	2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-10 and 12* is/are rejected.

7)☒ Claim(s) *4,5 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it is more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1-12 are objected to because of the following informalities:

In claim 1 line 2, it is suggested to delete "such".

In claim 1 line 5, it is suggested to change "a data communications link;" to --- the data communications link; ---.

In claim 1 line 12, it is suggested to change "over said link;" to --- over said data communications link ; ---.

In claim 1 lines 14, 15 and 18, it is suggested to change "the module" to --- the interface module ---.

In claim 1 line 19, it is suggested to change "the intra-node" to --- an intra-node ---.

In claim 2 line 1, it is suggested to change "An" to --- The ---. Similar problems exist in claim 3 line 1, claim 4 line 1, claim 5 line 1, claim 6 line 1, claim 9 line 1, claim 10 line 1, claim 11 line 1, and claim 12 line 1.

In claim 3 line 4, it is suggested to change "the port" to --- the external port ---.

In claim 3 line 5, it is suggested to change "for data communications" to --- for said data communications ---.

In claim 4 line it is suggested to change "of_said" to --- of said ---.

In claim 5 line 5, it is suggested to change "an internal port" to --- the internal port ---.

In claim 5 line 6, it is suggested to change "the module" to --- the interface module ---

In claim 6 line 2, it is suggested to change "one external port" to --- one of the plurality of external port ---.

In claim 7 line 3, it is suggested to delete "such".

In claim 7 line 5, it is suggested to change "a data communications link" to --- the data communications link ---.

In claim 7 line 12, it is suggested to change "said link;" to --- said data communications link; ---.

In claim 7 lines 14,15 and 18, it is suggested to change " the module" to --- the interface module ---.

In claim 7 line 19, it is suggested to change "the intra-node" to --- an intra-node ---.

In claim 8 line 10, it is suggested to change "over the link" to --- over the data communications link ---.

In claim 8 lines 11, 12 and 15, it is suggested to change "the module" to --- the interface module ---.

In claim 8 lines 16 and 20, it is suggested to change "each interface module" to --- said each interface module ---.

In claim 10 line 4, it is suggested to change "a plurality of the interface and switching modules" to --- the plurality of the interface modules and said switching modules ---.

In claim 11 line 2, it is suggested to change " each interface module" to --- said each interface module ---.

In claim 12 line 1, it is suggested to change "one switching node" to --- the switching node ---.

In claim 12 line 4, it is suggested to change "a plurality of the interface modules" to --- the plurality of the interface modules ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deneroff et al. (US 6,829,666) in view of Ganmukhi et al. (US 5,953,314).

As far as understood, with respect to claim 1, Deneroff et al. disclose modular computing architecture having common communication interface, comprising:

an external port for connection to a data communications link (figure 3, reference 1315, col. 7 lines 37-38);

a plurality of internal ports (figure 3, references 1325, 1330, 1340 and 1335) for connection to respective internal ports of said other interface modules of the switching node (col. 7 lines 20-25 and col. 7 lines 41-50);

a link interface (figure 3, reference 1335), connected to the external port (figure 3, reference 1315), for processing inbound data for forwarding across the switching node and outbound data for transmission over said link (col. 7 line 66 to col. 8 line 2);

a switch circuit (figure 13, reference 1350), connected between the link interface (figure 3, reference 1335) and the internal ports of the module (figure 3, references 1325, 1330, 1340 and 1335), for transmission of data between the internal ports of the module and between the internal ports and the link interface (col. 7 lines 51-53 and col. 7 lines 58-61); and

a controller (reference L1 system controller) for controlling routing of data via the internal ports of the module (col. 4 lines 7-11). However, Deneroff et al. do not expressly disclose a controller for controlling routing of data in accordance with an intra-node routing protocol governing routing of data across the intra-node network of interconnected interface modules of the switching node. In an analogous art, Ganmukhi et al. disclose a controller (figure 1, reference 12 or 14) for controlling routing of data in accordance with an intra-node routing protocol governing routing of data across the intra-node network of interconnected interface modules of the switching node (col. 2 lines 38-65).

One skilled in the art would have recognized a controller, and would have applied Ganmukhi et al.'s controller in accordance with an intra-node routing protocol governing routing of data across the intra-node network of interconnected interface modules of the switching node in Deneroff et al.'s L1 system controller. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Ganmukhi et al.'s control processor switchover for a telecommunications switch in Deneroff et al.'s modular computing architecture having common communication interface with the motivation being to provide a control processor card in conjunction with a switch fabric card to interconnect Input/Output ("I/O") cards and control switch operation (col. 1 lines 50-53).

For claim 2, Deneroff et al. disclose including a plurality of external ports (figure 13, references 1315 and 1310) for connection to respective data communications links, wherein

the link interface is connected to each of the external ports for processing said inbound and outbound data (col. 7 line 66 to col. 8 line 2).

For claim 3, Deneroff et al. disclose wherein the link interface comprises a communications adapter for format conversion between a link data format for the external port, for data communications over a link connected to the port in use, and a switch data format for data communications across the switching node (col. 7 line 66 to col. 8 line 2).

For claim 6, Deneroff et al. disclose including at least one external port (figure 3, reference 1315) which is connected or connectable directly to the switch circuit (col. 7 lines 58-61).

As far as understood, with respect to claim 7, Deneroff et al. disclose modular computing architecture having common communication interface, comprising:

an external port for connection to a data communications link (figure 3, reference 1315, col. 7 lines 37-38);

a plurality of internal ports (figure 3, references 1325, 1330, 1340 and 1335) for connection to respective internal ports of said other interface modules of the switching node (col. 7 lines 20-25 and col. 7 lines 41-50);

a link interface (figure 3, reference 1335), connected to the external port (figure 3, reference 1315), for processing inbound data for forwarding across the switching node and outbound data for transmission over said link (col. 7 line 66 to col. 8 line 2);

a switch circuit (figure 13, reference 1350), connected between the link interface (figure 3, reference 1335) and the internal ports of the module (figure 3, references 1325, 1330, 1340 and 1335), for transmission of data between the internal ports of the module (figure 3, references 1325, 1330, 1340 and 1335) and between the internal ports and the link interface (col. 7 lines 51-53 and col. 7 lines 58-61); and

a controller (reference L1 system controller) for controlling routing of data via the internal ports of the module (col. 4 lines 7-11). However, Deneroff et al. do not expressly disclose a controller for controlling routing of data in accordance with an intra-node routing protocol governing routing of data across the intra-node network of interconnected interface modules of the switching node. In an analogous art, Ganmukhi et al. disclose a controller (figure 1, reference 12 or 14) for controlling routing of data in accordance with an intra-node routing protocol governing routing of data across the intra-node network of interconnected interface modules of the switching node (col. 2 lines 38-65).

One skilled in the art would have recognized a controller, and would have applied Ganmukhi et al.'s controller in accordance with an intra-node routing protocol governing routing of data across the intra-node network of interconnected interface modules of the switching node in Deneroff et al.'s L1 system controller. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Ganmukhi et al.'s control processor switchover for a telecommunications switch in Deneroff et al.'s modular computing architecture having common communication interface with the motivation being to provide a control processor card in conjunction with a switch fabric card to interconnect Input/Output ("I/O") cards and control switch operation (col. 1 lines 50-53).

As far as understood, with respect to claim 8, Deneroff et al. disclose modular computing architecture having common communication interface, comprising:

each interface module (figure 13, reference 1300) comprises at least one external port (figure 3, reference 1315) for connection to a data communications link (col. 7 lines 37-38), a plurality of internal ports (figure 3, references 1325, 1330, 1340 and 1335), a link interface (figure 3, reference 1335), which is connected to said at least one external port (figure 3, reference 1315), for processing inbound data for forwarding across the switching

node and outbound data for transmission over the link (col. 7 line 66 to col. 8 line 2), a switch circuit (figure 3, reference 1350), which is connected between the link interface (figure 3, reference 1335) and the internal ports of the module (figure 3, references 1325, 1330, 1340 and 1335), for transmission of data between the internal ports of the module and between the internal ports and the link interface (col. 7 lines 51-53 and col. 7 lines 58-61), and a controller (reference L1 system controller) for controlling routing of data via the internal ports of the module (col. 4 lines 7-11); at least some of the internal ports of each interface module are connected to respective internal ports of one at least one other said interface module whereby the interface modules are connected in an intra-node network (col. 7 lines 20-25 and col. 7 lines 41-50).

However, Deneroff et al. do not expressly disclose wherein the controller of each interface module is arranged to control said routing of data in accordance with an intra-node routing protocol governing routing of data across said intra-node network. In an analogous art, Ganmukhi et al. disclose wherein the controller (figure 1, reference 12 or 14) of each interface module (figure 1, reference 16 and 18) is arranged to control said routing of data in accordance with an intra-node routing protocol governing routing of data across said intra-node network (col. 2 lines 38-65).

One skilled in the art would have recognized the controller of each interface module, and would have applied Ganmukhi et al.'s controller of each interface module is arranged to control said routing of data in accordance with an intra-node routing protocol governing routing of data across said intra-node network in Deneroff et al.'s L1 system controller. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Ganmukhi et al.'s control processor switchover for a telecommunications switch in Deneroff et al.'s modular computing architecture having common communication

interface with the motivation being to provide a control processor card in conjunction with a switch fabric card to interconnect Input/Output ("I/O") cards and control switch operation (col. 1 lines 50-53).

8. Claims 9-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deneroff et al. (US 6,829,666) in view of Ganmukhi et al. (US 5,953,314) further in view of Hauser et al. (US 5,983,260).

For claims 9-10 and 12, Deneroff et al. in view of Ganmukhi et al. do not expressly disclose wherein:

the switching node includes at least one switching module comprising a plurality of internal ports, a switch circuit for transmission of data between the internal ports of the switching module, and a controller for controlling routing of data via the internal ports of the switching module in accordance with said intra-node routing protocol; and

at least some of the internal ports of the switching module are connected to respective internal ports of one at least one said interface module, whereby the switching module is connected in said intra-node network.

In an analogous art, Hauser et al. disclose wherein:

the switching node (figure 1, reference 10) includes at least one switching module (figure 1, reference SCM 14, col. 2 lines 36-38) comprising a plurality of internal ports (figure 2, references 54 and 56, col. 4 lines 31-33), a switch circuit (figure 4, reference 34) for transmission of data between the internal ports of the switching module (col. 6 lines 27-33), and a controller (figure 3, reference MTC 30, col. 5 lines 29-32) for controlling routing of data via the internal ports of the switching module (figure 1, reference SCM 14) in accordance with said intra-node routing protocol (col. 3 lines 38-42 and col. 5 lines 32-40); and

at least some of the internal ports of the switching module (figure 4, reference SCM 14) are connected to respective internal ports of one at least one said interface module (figure 4, reference IOM 12), whereby the switching module (figure 4, reference SCM 14) is connected in said intra-node network (figure 4, col. 4 lines 31-47 and col. 6 lines 20-33).

Hauser et al. further disclose including a plurality of said switching modules (figure 4, references 14 and 16), wherein at least some of the internal ports of each switching module are connected to respective internal ports of a plurality of the interface and switching modules in the intra-node network (col. 3 lines 38-42 and col. 5 lines 32-40 as set forth in claim 10); at least one switching node (figure 4, reference 14), and a plurality of data communications links (figure 4, references 84 and 90), connected to respective external ports of a plurality of the interface modules (figure 4, reference IOM 12) of the switching node (figure 4, reference SCM 14), at least one of said data communications links connecting at least one network device to the switching node (col. 6 lines 5-33 as set forth in claim 12).

One skilled in the art would have recognized a switching module, and would have applied Hauser et al.'s switching module in Deneroff et al.'s modular computing system. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Hauser et al.'s serial control and data interconnects for coupling an I/O module with a switch fabric in a switch in Deneroff et al.'s modular computing architecture having common communication interface with the motivation being to provide modularity, scalability, redundancy, and improved fault isolation (col. 1 lines 53-54).

Allowable Subject Matter

9. Claim 4-5 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D Nguyen whose telephone number is 571-272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Nguyen

Toan Nguyen